Paper No. 28

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte YOUSEF A. KHALIDI and MOTI N. THADANI

Appeal No. 1999-2252
Application No. 08/780,790

ON BRIEF

Before FLEMING, GROSS, and DIXON, ***Administrative Patent Judges.***

FLEMING, ***Administrative Patent Judge***.

DECISION ON APPEAL

This is an appeal from the final rejection of claims 1-11, 13-14, and 16-22, all of the claims pending in the present application. Claims 12 and 15 have been canceled. The invention relates to a computer system (figure 2, item 100; specification, page 6, lines 10-12, and page 7, lines 14-16) supporting data transfers without copying unmodified data

(figure 2, item 270) between a memory object (figure 2, item 125) associated with a fast buffer (figure 2, item 115) and a sink device (figure 2, item 130). The computer system comprises a processor (figure 2, item 160; specification, page 6, lines 21-22), a main memory (figure 2, item 110), a source (figure 2, item 120), and a sink (figure 2, item 130). The main memory comprises an application instructions storage (figure 2, item 180; specification, page 6, lines 12-19), an operating system instructions storage (figure 2, item 170), and a fast buffer (figure 2, item 115). The source comprises a memory object (figure 2, item 125). A buffer mapping (figure 1, item 140) establishes an association between the memory object and the fast buffer.

When the data are not modified, the memory object is transferred from the source to the sink via a first data path data transfer (figure 1, item 150; specification, page 6, lines 22-23). When the data are partially modified, the data are transferred from the source to the sink via two data paths. A first data path (figure 2, item 270) is used for unmodified data and a second path (figure 2, item 250) is used for modified data. The unmodified data path transfers data

directly from the memory object to the sink. The modified data path transfers data from the fast buffer to the sink (specification, page 8, lines 25-27 and page 9, lines 1-2).

Independent claim 1 is reproduced as follows:

1. A method for controlling data transfer, the method comprising the steps of:

(A) requesting by an application that an operating system establish an association for purposes of data transfer between a fast buffer and a memory object storing the data on a source device;

(B) establishing by the operating system the association between the fast buffer and the memory object;

(C) directing by the application that the data of the memory object associated with the fast buffer be transferred to a sink device via a first data path without copying any portion of the data to main memory unless the application attempts to access via a memory fetch/store, any portion of the transferring data and

(D) copying the data to main memory prior to transfer to the sink device along a second data path when the application modifies the data of the memory object prior to step (C).

The Examiner relies on the following references:

Aichelmann et al. (Aichelmann)	4,823,259	Apr. 18, 1989
Dong et al. (Dong)	5,093,912	Mar. 3, 1992
Amini et al. (Amini)	5,381,538	Jan. 10, 1995

Appellants' admitted prior art which includes the Druschel et al. (Druschel) article titled "Fbufs: A High-Bandwidth Cross-

Domain Transfer Facility", 14th ACM Symposium on Operating Systems Principles, pages 189-202 (December 1993), and the Krieger et al. (Krieger) article titled "The Alloc Stream Facility: A Redesign of Application-Level Stream I/O," Computer, Vol. 27, No. 3, pages 75-82 (March 1994).

Claims 1-2, 4-7, 9-11, 13, 14 and 16 stand rejected under 35 U.S.C. § 103 as being unpatentable over Appellants' admitted prior art in view of Aichelmann.

Claims 17-20 stand rejected under 35 U.S.C. § 103 as being unpatentable over Appellants' admitted prior art in view of Aichelmann and Dong.

Claims 21 and 22 stand rejected under 35 U.S.C. § 103 as being unpatentable over Appellants' admitted prior.

Claims 3 and 8 stand rejected under 35 U.S.C. § 103 as being unpatentable over Appellants' admitted prior art in view of Aichelmann and Amini.

Rather than reiterate the arguments of Appellants and the Examiner, reference is made to the Brief[1] and the Examiner's Answer[2] for the respective details thereof.

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[1] The Brief was received February 1, 1999, and a Supplementary Appeal Brief was received August 13, 2001. The Supplementary Appeal Brief will be referred to herein as the "brief."

[2] The Examiner's Answer was mailed March 2, 1999.

OPINION

A. Rejection of claims 1-2, 4-7, 9-11, 13, 14 and 16 under 35 U.S.C. § 103 as being unpatentable over Appellants' admitted prior art in view of Aichelmann.

We will not sustain the rejection of Claims 1-2, 4-7, 9-11, 13, 14 and 16 stand rejected under 35 U.S.C. § 103.

The Examiner has failed to set forth a ***prima facie*** case. It is the burden of the Examiner to establish why one having ordinary skill in the art would have been led to the claimed invention by the express teachings or suggestions found in the prior art, or by implications contained in such teachings or suggestions. ***In re Sernaker***, 702 F.2d 989, 995, 217 USPQ 1, 6 (Fed. Cir. 1983).

Appellants argue[3] that the cited references do not disclose, suggest, or render obvious (i) an application directing the data in a memory object associated with a fast buffer be transferred to a sink device without copying any portion of the data to the main memory unless the application

[3] Brief, page 6.

attempts to access via a memory fetch/store any portion of the transferring data, and

(ii) a first data path connecting a memory object, which is associated with a fast buffer, to a sink device for the purpose of data transfer.

In particular, Appellants argue[4] that Druschel's operating system facility data objects are copied to, or filled in, the fast buffers for data transfer[5] without determining whether or not the data have been modified. In addition, Appellants argue[6] that Krieger also requires[7] a copying to buffer, which is allocated in the main memory, be performed for data transfer without determining whether or not the data have been modified. In regard to Aichelmann, Appellants argue[8] that the data paths disclosed by this reference are not between a

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[4] Brief, pages 7-8.

[5] See Druschel, page 194, right column, section 3.2.2, second paragraph; page 195, left column, first full paragraph, and section 3.2.4, third paragraph.

[6] Brief, page 9.

[7] Krieger, page 80, left column, and middle column, first partial paragraph.

[8] Brief, pages 9-10.

source device and a sink device which are input/output devices, and that this reference does not disclose or suggest a first data path between a memory object and a sink device. Appellants then contrast this disclosure to their invention, which requires a first data path linking the source device to the sink device without going through main memory or a cache subsystem.

In response to the Examiner's statement[9] that "[t]hese rather slight system call variations would have been obvious to one skilled in the art," Appellants argue[10] that the cited references do not expressly or implicitly suggest these aspects of their invention. In addition, Appellants argue that the Examiner failed to present a convincing line of reasoning as to why a combination of admitted prior art and Aichelmann is an obvious improvement of a fast buffer to transfer data via a first data path, without copying any portion of the data to main memory.

[9] Answer, page 4, lines 3-4.

[10] Brief, pages 6-7.

The Examiner argues[11] that Druschel teaches that fast buffers can be used to optimize the transfer of data that originates and/or terminates at an I/O device. In addition, the Examiner finds[12] that in view of the read2 and write2 call variations "all the elements of this method claim are satisfied

. . . and consequently satisfying such a claim would have been obvious to one skilled in the art."

The Examiner then points to Krieger[13] as showing the "last limitation" of claim 1.

The Examiner then asserts[14] that Aichelmann teaches the transfer of data along a first data path and along an alternate second data path and finds:

> "It would have been obvious to one of ordinary skill in the art at the time the invention was made to improve upon the system taught by Applicant's admitted prior art by implementing the improvements

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[11] Answer, page 3.

[12] Answer, page 4.

[13] Page 77, left column, paragraph 2; page 76, right column, last paragraph; page 78, right column, paragraph 2; page 80, middle column, last paragraph.

[14] Answer, page 4.

> detailed above because it would provide the system taught by Applicant's admitted prior art with the enhanced capability of a more efficient (i.e., faster) transfer of data . . . ."

Finally, the Examiner states[15] "it would be obvious to a programmer of ordinary skill to effect a direct memory transfer between any desired source and destination, as opposed to performing a copy operation to an intermediate memory, as the realized enhanced transfer efficiency is self evident."

Turning first to Appellants' claim 1, we find that the final subparagraph of this claim provides[16]

> "directing by the application that the data of the memory object associated with the fast buffer be transferred to a sink device via a first data path without copying any portion of the data to main memory unless the application attempts to access via a memory fetch/store, any portion of the transferring data."

Similarly, claim 6 recites[17]

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[15] Answer, pages 10-11.

[16] Lines 8-12.

[17] Lines 8-12.

"a writer adapted to permit the application to direct that the data of the memory object associated with the fast buffer be transferred to a sink device along a first data path without copying the data into main memory along a second data path unless the application attempts to access via a memory fetch/store, any portion of the transferring data."

We agree with Appellants that neither Druschel or Krieger teach this limitation.

Druschel teaches[18] that when a PDU arrives from the network "An fbuf is allocated in the kernel, filled, and then transferred . . ." (emphasis added). In addition, Druschel teaches[19] "The optimization integrates buffer management and cross-domain data transfer facility by placing the entire aggregate object into fbufs" (emphasis added). Druschel therefore requires copying to fbuf for data transfer without determining whether or not the data has been modified.

Krieger teaches[20] that for the interface modules the I/O read algorithm requires "Read first calls salloc to . . ., then copies the data from the allocated region to the user specified buffer" (emphasis added). In addition, Krieger

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[18] Page 194, section 3.2.2.

[19] Page 195, section 3.2.3.

[20] Page 80, left column.

teaches[21] that the major advantage of using ASI as the interface is that "[d]ata is copied from the library to the application buffer with the stream unlocked, [sic] allowing for greater concurrency . . ." (Emphasis added). Krieger therefore requires copying of data to the buffer.

Although Krieger states[22] "[d]ata copying occurs only when the application transforms the data between the system input and output buffers," this copying is between buffers or allocated memory regions, and not copying of data from a source device external to main memory, to the fast buffer in main memory, as claimed.

In addition, the Examiner has made the following three statements directed to the aspects of the invention found obvious and the reasons why they were obvious. First, that read()/write() calls which are used to transfer data between a device and an application program resident memory location "could be modified to take an operating system resident fast buffer argument (representation) as opposed to an application

[21] Page 80, middle column.

[22] Page 77, left column; figure 1(c).

resident buffer argument . . . These rather slight system call variations would have been obvious to one skilled in the art." Answer, page 4. Second, that

> It would have been obvious to one of ordinary skill in the art at the time the invention was made to improve upon the system taught by **Applicant's admitted prior art** by implementing the improvements detailed above because it would provide the system taught by **Applicant's admitted prior art** with the enhanced capability of a more efficient (i.e., faster) transfer of data. Answer, pages 4-5.

Third, that " . . . it would be obvious to a programmer of ordinary skill to effect a direct memory transfer between any desired source and destination, as opposed to performing a copy operation to an intermediate memory, as the realized enhanced transfer efficiency is self evident." Answer, page 10.

The Federal Circuit states that "[t]he mere fact that the prior art may be modified in the manner suggested by Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." ***In re Fritch***, 972 F.2d 1260, 1266 n.14, 23 USPQ2d 1780, 1783-84 n. 14 (Fed. Cir. 1992), ***citing In re Gordon***, 733 F.2d 900, 902,

221 USPQ 1125, 1127 (Fed. Cir. 1984). However, "[o]bviousness may not be established using hindsight or in view of the teachings or suggestions of the invention." ***Para-Ordnance Mfg. v. SGS Importers Int'l***, 73 F.3d at 1087, 37 USPQ2d at 1239, ***citing W.L. Gore & Assocs., Inc. v. Garlock, Inc***. 721 F.2d at 1553, 220 USPQ at 312-13.

We agree with Appellants that the Examiner has failed to set forth a ***prima facie*** case. The Examiner must establish why one having ordinary skill in the art would have been led to the claimed invention by the express teachings or suggestions found in the prior art, or by implications contained in such teachings or suggestions. The references of record fail to provide express teachings or suggestions to make the combinations suggested by the Examiner.

Therefore, we will not sustain the rejection of Claims 1-2, 4-7, 9-11, 13, 14 and 16 stand rejected under 35 U.S.C. § 103 as being unpatentable over Appellants' admitted prior art in view of Aichelmann.

B. Rejection of claims 17-20 under 35 U.S.C. § 103 as unpatentable over Appellants' admitted prior art in view of Aichelmann and Dong.

Claims 17-20 stand rejected under 35 U.S.C. § 103 as being unpatentable over Appellants' admitted prior art in view of Aichelmann and Dong.

We note that although the Examiner cites the Dong reference in the first sentence of this rejection, the Examiner's Answer, the final rejection, and the Office action immediately preceding the final rejection,[23] fail to further mention Dong or point to any specific sections of this reference relied upon by the Examiner for this rejection.

Our analysis of claim 17 reveals that this claim recites at lines 5-7 substantially the same limitations of claim 1, subparagraph (C), we analyzed above[24] and found lacking in Druschel, Krieger and Aichelmann. Our analysis of Dong shows this reference discloses the management of a buffer pool to achieve efficient use of resources, and not the claim

[23] Paper No. 15.

[24] Page 8.

limitations in lines 5-7 of claim 17. The general statements[25] by the Examiner in regard to this rejection do not address these claim limitations.

Therefore, we will not sustain the rejection of Claims 17-20 under 35 U.S.C. § 103 as being unpatentable over Appellants' admitted prior art in view of Aichelmann and Dong.

C. Rejection of claims 21 and 22 under 35 U.S.C. § 103 as unpatentable over Appellants' admitted prior art.

Claims 21 and 22 stand rejected under 35 U.S.C. § 103 as being unpatentable over Appellants' admitted prior.

Appellants argue[26] that the cited references do not teach, suggest, or render obvious (I) a data transfer method involving a computer system having application and operating system instructions stored in main memory, and (ii) the data of the memory object associated with the fast buffer being transferred to a sink device without storing the data in the main memory during transfer.

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[25] Answer, page 6.

[26] Brief, page 11.

The Examiner asserts[27] that "[i]t is well known that computer systems, such as UNIX, have application and operating system instructions stored in main memory . . . ." In addition the Examiner relies upon the arguments presented by the Examiner in regard to claim 1.

As we have determined above[28] that the "admitted prior art" does not disclose a data transfer from a source device to a sink device without copying data to a main memory, finding that both Druschel and Krieger both require copying to buffer, we find that the admitted prior art fails to teach or suggest the limitations recited by the last paragraph of claims 21 and 22.

Furthermore, although Appellants have not traversed the Examiner's statement[29] that it is well known that computer systems, such as UNIX, have application and operating system instructions stored in main memory, Appellants have argued that the prior art does not suggest or render obvious a data

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[27] Answer, page 5.

[28] Pages 8 and 9.

[29] Answer, page 5.

transfer method involving a computer system having application and operating system instructions stored in main memory. The Examiner has not addressed this argument.

We therefore agree with Appellants that the Examiner has failed to set forth a ***prima facie*** case. The Examiner must establish why one having ordinary skill in the art would have been led to the claimed invention by the express teachings or suggestions found in the prior art, or by implications contained in such teachings or suggestions. The references of record fail to provide express teachings or suggestions to make the combinations suggested by the Examiner.

Therefore, we will not sustain the rejection of Claims 21-22 under 35 U.S.C. § 103 as being unpatentable over Appellants' admitted prior art.

D. Rejection of claims 3 and 8 under 35 U.S.C. § 103 as unpatentable over Appellants' admitted prior art in view of Aichelmann and Amini.

Claims 3 and 8 stand rejected under 35 U.S.C. § 103 as being unpatentable over Appellants' admitted prior art in view of Aichelmann and Amini.

Although Appellants have failed to specifically argue these claims, Appellants include[30] these dependent claims in their list of appealed claims.

We note that although the Examiner cites the Amini reference in the first sentence of this rejection, the Examiner's Answer, the final rejection, and the Office action immediately preceding the final rejection,[31] do not mention Amini or point to any specific section of this reference relied upon by the Examiner for this rejection.

Claim 3 depends upon claim 1, and claim 8 depends upon claim 6. Our analysis of Amini shows this reference disclosing a DMA controller relevant to the additional claim limitations presented in dependent claims 3 and 8, and not the claim limitations we found above to be in claims 1 and 6 and not in Druschel, Krieger and Aichelmann.

The statements by the Examiner in regard to this rejection do not address the limitations found lacking in claims 1 and 6. Therefore, we will not sustain the

[30] Brief, page 3, section III.

[31] Paper No. 15.

rejection of Claims 3 and 8 under 35 U.S.C. § 103 as being unpatentable over Appellants' admitted prior art in view of Aichelmann and Amini.

We have not sustained the rejection of claims 1-11, 13-14 and 16-22 under 35 U.S.C. § 103. Accordingly, the Examiner's decision is reversed.

REVERSED

MICHAEL R. FLEMING)

Administrative Patent Judge	)
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	)
	) BOARD OF PATENT
ANITA PELLMAN GROSS	) APPEALS
Administrative Patent Judge	) AND
	) INTERFERENCES
	)
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	)
JOSEPH L. DIXON	)
Administrative Patent Judge	)

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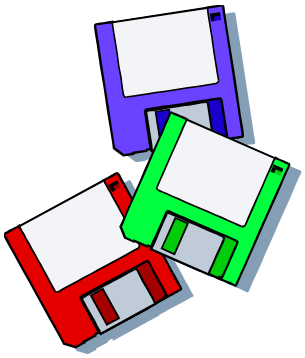

Lesley

Appeal No. 1999-2252
Application No. 08/780,790

APJ FLEMING

APJ GROSS

APJ DIXON

DECISION: REVERSED

Prepared: July 29, 2002

Draft Final

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